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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/699,537	10/30/00	MODEN	W 2687.3US (9

EXAMINER	
BROCK, T. P.	
ART UNIT	PAPER NUMBER
2815	

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JAMES R. DUZAN
TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY UT 84110

DATE MAILED:
09/17/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/699,537	MODEN, WALTER L.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features claimed in claims 17 – 24 and 40 – 49 such as "providing a board having a die side surface... a plurality of bond pads located on the die side surface...connecting said plurality of bond pads of said semiconductor die to said plurality of bond pads of the board using a plurality of wire bonds;" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 17 – 25 and 40 – 50 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where in the originally filed specification support for an embodiment of the present invention that has wire bonds that connect bond pads of a die to bond pads of a board that do not go through a via in the board exists.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 23, 24, 48 and 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear how a sealant would fill the vias of the embodiments claimed in claims 20 and 45 because it appears that the sealant is used for protecting wires which connect a chip mounted on a die side surface of a board to bond pads on a second attachment surface of the board. The embodiments in claims 20 and 45 do not have this feature, but the apparent use of vias in these claims are to electrically connect a plurality of electrical connectors on a second attachment surface of a board to bond pads on a die side surface of the board.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 – 16 and 26 – 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al. (USPAT 5674785, Akram) in view of Kohno et al. (USPAT 5293068, Kohno).

Akram discloses in figures 5 – 6 a method of electrically connecting a semiconductor die to a substrate.

With regard to claim 1, Akram discloses in figures 5 – 6 providing a semiconductor die (18) having a surface having a plurality of bond pads thereon (24). Akram discloses in figures 5

– 6 providing a substrate (12b and 12c) having a die side surface, a second attachment surface, at least one via (20b) extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits (14), and a plurality of connection points located on the second attachment surface of the substrate. Akram discloses in figures 5 – 6 attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of the substrate. Akram discloses in figures 5 – 6 connecting the plurality of bond pads of the semiconductor die to the plurality of connection points of the substrate using a plurality of wire bonds (32), the plurality of wire bonds extending through the at least one via extending through the substrate. Akram does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads of Kohno as the connection points of Akram in order to have a dedicated surface in which to bond a wire to as is well known in the art.

With regard to claim 2, it is inherent in the method of Akram that an adhesive is applied to a portion of the die side of the substrate to attach the semiconductor die thereto.

With regard to claim 3, Akram discloses in figure 6 filling at least a portion of the via in the substrate with a sealant (36b).

With regard to claim 4, Akram discloses in figure 6 filling the via in the substrate with a sealant (36b).

With regard to claim 5, Akram discloses in figures 1 and 3a providing a semiconductor die (18) having a plurality of bond pads (24) thereon. Akram discloses in figure 1 providing a master board (30) inherently having a plurality of circuit traces thereon. Akram discloses in

figure 1 providing a board (12) having a die side surface, a second attachment surface, at least one via (20) extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of connection points located on the second attachment surface of the board. Akram discloses in figure 1 providing a plurality of electrical connectors (16) for connecting the plurality of connection points located on the second attachment surface of the board to the circuit traces of the master board. Akram discloses in figure 1 attaching the semiconductor die to a portion of the die side surface of the board. Akram discloses in figure 2 connecting the plurality of bond pads of the semiconductor die to the plurality of connection points of the board using a plurality of wire bonds, the plurality of wire bonds extending through the at least one via extending through then board. Akram discloses in figure 3a connecting the board and master board using the plurality of electrical connectors on the board to the plurality of circuit traces on the master board. Akram does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads of Kohno as the connection points of Akram in order to have a dedicated surface in which to bond a wire to as is well known in the art.

With regard to claim 6, Akram discloses in figure 1a that the board could include a plurality of vias extending therethrough.

With regard to claim 7, Akram discloses in figure 1 that the plurality of electrical connectors comprise solder balls.

With regard to claim 8, Akram discloses in figure 9 a method of electrically connecting at least two semiconductor die to a substrate. Akram discloses in figure 9 providing at least two

semiconductor die (18), each semiconductor die having a surface inherently having a plurality of bond pads. Akram discloses in figure 9 providing a substrate (12m) having a die side surface, a second attachment surface, at least tow vias extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits (14), and a plurality of connection points located on the second attachment surface of the board. Akram discloses in figure 9 attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the substrate having the plurality of bond pads of the semiconductor die located over one of the at least two vias extending through the substrate. Akram discloses in figure 9 connecting the plurality of bond pads of the semiconductor die to the plurality of connection points of the substrate using a plurality of wire bonds, the plurality of wire bonds extending through the one via extending through the substrate of the at least two vias extending through the substrate. Akram does not disclose that the connection points are bond pads. Kohno discloses in figure 4 bond pads on a second attachment surface of a substrate (2). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bond pads of Kohno as the connection points of Akram in order to have a dedicated surface in which to bond a wire to as is well known in the art.

With regard to claim 9, it is inherent that Akram applies an adhesive to a portion of the die side of the substrate to attach each semiconductor die thereto.

With regard to claims 10 and 11, Akram does not show a sealant in the vias of the embodiment discloses in figure 9. Akram does show a sealant filling the vias in the embodiment shown in figure 6. It is obvious that Akram could fill a portion or all of each via in the substrate

with a sealant as done in the embodiment disclosed in figure 6 in order to secure the wires of the embodiment in claim 9 and make the package more durable.

With regard to claim 12, similar to the embodiments disclosed by Akram as applied to claim 8 above, Akram does not disclose a master board in figure 9. Akram does disclose attaching a semiconductor die to a master board in figure 3a and similar to the rejection of claim 5 above. It would have been obvious to one of ordinary skill in the art that electrical connectors (16) shown in figure 9 are used for connecting the plurality of semiconductor die to a master board as shown in figure 3a of Akram.

With regard to claim 13, Akram discloses in figure 9 that the plurality of electrical connectors comprise solder balls.

With regard to claim 14, Akram does not disclose that the plurality of electrical connectors comprise pins. Pins are well known in the art. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use pins to connect the plurality of semiconductor die to a master board of Akram in order to make an electrical connection between the die and board as is well known in the art.

With regard to claims 15 and 16, they are rejected similar to claims 10 and 11.

Claims 26 – 41 are rejected similar to claims 1 – 16 respectively since the use of the term "at least one" is covered under the definition of "a plurality".

8. Claims 17 – 19 and 42 – 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okinaga et al. (USPAT 5107329, Okinaga) in view of Mahulikar et al. (USPAT 6262477, Mahulikar).

With regard to claim 17, Okinaga discloses in figure 1 providing a semiconductor die (4) having a plurality of bond pads thereon. Okinaga discloses in figure 1 providing a master board (1) having a plurality of connection points (10) thereon. Okinaga discloses in figure 1 providing a board (3) having a die side surface, a second attachment surface, at least one via (8) extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the die side surface of the board. Okinaga discloses in figure 1 providing a plurality of electrical connectors (9) for connecting the plurality of bond pads located on the die side surface of the board to the connection points of the master board. Okinaga discloses in figure 1 attaching the semiconductor die to a portion of the die side surface of the board. Okinaga discloses in figure 1 connecting the plurality of bond pads of the semiconductor die to a plurality of bond pads of the board using a plurality of wire bonds (7). Okinaga discloses in figure 1 connecting the board and master board using the plurality of electrical connectors on the board to the plurality of connection points on the master board. Okinaga does not disclose that the connection points are circuit traces. Mahulikar discloses in figure 15 a plurality of connection points (112) that are circuit traces. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the circuit traces of Mahulikar in the method of Okinaga in order to connect the vias of the board to a ground or power circuit as taught by Mahulikar in column 8, lines 9 – 11.

With regard to claim 18, Okinaga discloses in figure 1 the board includes a plurality of vias extending therethrough.

With regard to claim 19, Okinaga discloses in figure 1 wherein the plurality of electrical connectors comprise wire bonds (9).

Claims 42 – 44 are rejected similar to claims 17 – 19 respectively since the use of the term "at least one" is covered under the definition of "a plurality".

9. Claims 20 – 22, 25, 45 – 47 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okinaga in view of Mahulikar and Yoneda et al. (USPAT 5615089, Yoneda).

With regard to claim 20, Okinaga discloses in figure 1 providing a semiconductor die (4) having a plurality of bond pads thereon. Okinaga discloses in figure 1 providing a master board (1) having a plurality of connection points (10) thereon. Okinaga discloses in figure 1 providing a board (3) having a die side surface, a second attachment surface, a plurality of vias (8) extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the die side surface of the board. Okinaga discloses in figure 1 providing a plurality of electrical connectors (9) for connecting the plurality of bond pads located on the die side surface of the board to the connection points of the master board. Okinaga discloses in figure 1 attaching the semiconductor die to a portion of the die side surface of the board. Okinaga discloses in figure 1 connecting the plurality of bond pads of the semiconductor die to a plurality of bond pads of the board using a plurality of wire bonds (7). Okinaga discloses in figure 1 connecting the board and master board using the plurality of electrical connectors on the board to the plurality of connection points on the master board. Okinaga does not disclose that the connection points are circuit traces. Mahulikar discloses in figure 15 a plurality of connection points (112) that are circuit traces. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the circuit traces of Mahulikar in the method of Okinaga in order to connect the vias of the board to a

ground or power circuit as taught by Mahulikar in column 8, lines 9 – 11. Okinaga and Mahulikar do not disclose a plurality of semiconductor die. Yoneda discloses in figure 3 providing a plurality of semiconductor die (23) on a board. It would have been obvious to one of ordinary skill in the art to use a plurality of semiconductor die such as Yoneda, in the method of Okinaga and Mahulikar, in order to mount many semiconductor chips on a common package substrate, without excessively reducing the pitch of the leads used for external connection as stated by Yoneda in column 2, lines 42 – 48.

With regard to claim 21, Okinaga discloses in figure 1 wherein the plurality of electrical connectors comprise wire bonds (9).

With regard to claim 22, Okinaga discloses in figure 1 wherein the plurality of electrical connectors comprise pins (9).

With regard to claim 25, Okinaga discloses in figure 1 applying an adhesive to a portion of the die side surface to attach each semiconductor die thereto.

Claims 45 – 47 and 50 are rejected similar to claims 20 – 22 and 25 respectively since the use of the term "at least one" is covered under the definition of "a plurality".

10. Claims 23, 24, 48 and 49 rejected under 35 U.S.C. 103(a) as being unpatentable over Okinaga, Mahulikar and Yoneda as applied to claims 20 and 45 above, and further in view of Akram.

As best the examiner can ascertain, it would have been obvious to combine Akram with Okinaga, Mahulikar and Yoneda in order to fill the vias with sealant to protect wires.

Response to Arguments

11. Applicant's arguments filed 8-6-2001 have been fully considered but they are not persuasive.

12. In response to applicant's argument that "...Applicant submits that Fig. 4 of Kohno does not disclose bond pads.", a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art.

13. Applicant's arguments with respect to claims 17 – 25 and 40 – 50 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Oh, Degani et al., Jones et al., Lin, Ackermann et al., Lin et al. and Chia et al. disclose mounting a die onto a board with vias therethrough onto a master board.

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
September 10, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800